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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,198	07/28/2003	Young-Joon Park	TI-35623	6116

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EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/628,198	PARK ET AL.
	Examiner	Art Unit
	Ginette Peralta	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8* is/are rejected.

7)☒ Claim(s) *2 and 4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 7, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (U. S. Pat. 6,709,970 B1).

Regarding claim 1, Park et al. discloses a method of manufacturing copper interconnects on a semiconductor wafer that comprises forming a layer 50 of patterned dielectric material, the patterned dielectric material defining spaces for the copper interconnects (as taught in col. 4, lines 55-67, and in Fig. 2); depositing a copper seed layer 90 over the layer of patterned dielectric material (as taught in col. 5, lines 10-14, 23-30, and in Fig. 4); depositing a first layer of copper grains 110 having a first initial grain size (as taught in col. 5, lines 51-54) over the copper seed layer by an electroplating process (as taught in col. 5, lines 31-48,and in Fig. 7); and depositing a second layer 130 of copper having a second initial grain size over the first layer of copper, the second layer of copper grains being deposited by an electroplating process (as taught in col. 6, lines 30-48, and in Fig. 8.)

Regarding claim 3, Park et al. discloses in col. 6, lines 30-32 that the second initial grain size is larger than the first initial grain size.

Regarding claim 7, Park et al. discloses a method of manufacturing copper interconnects on a semiconductor wafer that comprises forming a layer 50 of patterned dielectric material, the patterned dielectric material defining spaces for the copper interconnects (as taught in col. 4, lines 55-67, and in Fig. 2); depositing a copper seed layer 90 over the layer of patterned dielectric material (as taught in col. 5, lines 10-14, 23-30, and in Fig. 4); depositing a first layer of copper grains 110 having a first initial grain size (as taught in col. 5, lines 51-54) over the copper seed layer by an electroplating process (as taught in col. 5, lines 31-48,and in Fig. 7); and depositing at least one additional layer 130 of copper grains of differing initial grain size over the first layer of copper, the at least one additional layer of copper grains being deposited by an electroplating process (as taught in col. 6, lines 30-48, and in Fig. 8.)

Regarding claim 8, Park et al. discloses a method of manufacturing copper interconnects on a semiconductor wafer that comprises forming a layer 50 of patterned dielectric material, the patterned dielectric material defining spaces for the copper interconnects (as taught in col. 4, lines 55-67, and in Fig. 2); depositing a copper seed layer 90 over the layer of patterned dielectric material (as taught in col. 5, lines 10-14, 23-30, and in Fig. 4); depositing a first layer of copper grains 110 having a first initial grain size (as taught in col. 5, lines 51-54) over the copper seed layer by an electroplating process (as taught in col. 5, lines 31-48,and in Fig. 7); and depositing a second layer 130

of copper having a second initial grain size over the first layer of copper, the second layer of copper grains being deposited by an electroplating process (as taught in col. 6, lines 30-48, and in Fig. 8); and annealing the semiconductor wafer (as taught in col. 5, lines 49-50.)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. in view of Uzoh et al. (U. S. Pat. 6,861,354 B2)

Park et al. discloses a method of manufacturing copper interconnects on a semiconductor wafer that comprises forming a layer 50 of patterned dielectric material, the patterned dielectric material defining spaces for the copper interconnects (as taught in col. 4, lines 55-67, and in Fig. 2); depositing a copper seed layer 90 over the layer of patterned dielectric material (as taught in col. 5, lines 10-14, 23-30, and in Fig. 4); depositing a first layer of copper grains 110 having a first initial grain size (as taught in col. 5, lines 51-54) over the copper seed layer by an electroplating process (as taught in col. 5, lines 31-48,and in Fig. 7); and depositing a second layer 130 of copper having a

second initial grain size over the first layer of copper, the second layer of copper grains being deposited by an electroplating process (as taught in col. 6, lines 30-48, and in Fig. 8), and annealing the semiconductor wafer as disclosed in col. 5, lines 49-50.

Park et al. discloses the claimed invention with the exception of annealing the semiconductor wafer after the step of depositing a second layer of copper grains.

Uzoh et al. discloses a method of manufacturing copper interconnects on a semiconductor wafer that comprises forming a layer of patterned dielectric material 104, the patterned dielectric material defining spaces for the copper interconnects(col. 4, lines 44-47); depositing a copper seed layer 112 over the layer of patterned dielectric material (col. 4, lines 51-56); filling the patterned dielectric layer with copper (col. 4,lines 40-44); and annealing the semiconductor wafer after the deposition of the copper layer is completed, wherein the semiconductor wafer is annealed after the completed deposition of the copper layer for the disclosed intended purpose that annealing the structure after an initial chemical mechanical polishing step results in a stabilized structure and minimizing the tensile stress on the plated structures.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the semiconductor wafer of Park et al. after the step of depositing a second layer of copper grains, and even after the copper interconnects are filled for the disclosed intended purpose of Uzoh et al. of annealing the structure after an initial chemical mechanical polishing step results in a stabilized structure and

minimizing the tensile stress on the plated structures that is characteristic of the copper interconnects.

Regarding claim 6, Park et al., as modified by Uzoh et al. in col. 4, lines 28-32, discloses that the annealing step is performed within a temperature range of 150 to 420°C for a time between 5 to 300 seconds.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to vary the temperature and time of annealing as there is no statement denoting the criticality of the temperature and time of annealing and since the range of temperatures and range of time disclosed by Park et al. as modified by Uzoh et al. overlap with the ranges claimed by the inventors.

"In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.)" (MPEP 2144.04)

Response to Arguments

5. Applicant's arguments filed 12/6/04 have been fully considered but they are not persuasive.

Regarding applicant's argument that Park et al. teaches away from the claimed invention by teaching a second Cu layer formed by electroplating, CVD, or sputtering over a thin Cu layer but not over a first layer of copper grains as claimed, it is noted that the second copper layer 130, is deposited over a first layer of copper grains 110, as

disclosed in col. 5, lines 51-54) and furthermore, the layer 110 is deposited by electroplating, the layer which is deposited by CVD or sputtering is the copper seed layer 90 as taught in col. 2, lines 44-48, where it reads: "The **first and the second metal film** may be deposited using an electroplating process or an electroless plating process. The **seed metal film** may be deposited using a CVD process or a sputtering process." (Emphasis added)

Regarding applicant's argument that Park et al. teaches an annealing step following the deposition of the first layer of Cu grains, and that since the second Cu layer is not deposited over a first layer of copper grains, it is noted that Park et al. discloses in col. 5, lines 50-54, that the annealing step is performed to increase the grain size of the first layer of copper grains not to eliminate the grains, thus the second layer of copper grains is still formed over a first layer of copper grains.

Regarding applicant's argument that Park et al. teaches that the first layer of copper grains is annealed and then a second layer of copper grains is deposited and that it does not encompass the teachings of depositing a first layer of copper grains and the deposition of a second layer of copper grains on the first layer of copper grains, it is noted that the claim language does not preclude the annealing step prior to the deposition of the second layer of copper grains, furthermore although the first layer of copper grains is annealed, the second layer of copper grains is still indeed deposited over the first layer of copper grains.

Allowable Subject Matter

6. Claims 2 and 4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the allowance of the claims is the inclusion of the feature of depositing at least one additional layer of copper grains of any initial grain size over the second layer of copper grains, the at least one additional layer of copper grains being deposited by an electroplating process, which is not anticipated nor rendered obvious over the prior art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571) 272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GP

Wael Fahmy
SPE 2814